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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2706	(726/21,26,30).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2008/11/09 22:35
L2	3011	(713/166,193).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2008/11/09 22:35
L3	4561	(711/162,163).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2008/11/09 22:36
L4	430	(710/261,269).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2008/11/09 22:36
L5	1350	arm.as.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:37
L6	10278	L1 or L2 or L3 or L4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:41
L7	8	L6 (exception)same (vector)near(table). clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:42
L8	3	L5 (exception)same (vector)near(table). clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:42
L9	38	L6 (secure)same(non \$secure or insecure) same(mode).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:43
L10	16	L6 (secure)same(non \$secure or insecure) same(mode).clm. (exception or handl\$4). clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:43

L11	124	L6 (secure)same(non\$secure or insecure) same(mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:43
L12	25	L11 (exception)same (vector)near(table)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:44
L13	44	L7 or L9 or L12	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:44
L14	11	L13 ((exception)same (vector or table)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:44
L15	7	L14 (secure or mode) same(non\$secure or insecure)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:45
L16	10	"7165135".pn. "7237081".pn. "6363463".pn. "5561788".pn. "7171539".pn. "7117284".pn. "7305712".pn. "20040139346".pn. "20040153672".pn. "20030126520".pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/11/09 22:55
L17	7	L16 (exception)same (vector)near(table)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:55
L18	8	L16(secure)same(non\$secure or insecure) same(mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:55
L19	6	L17 L18	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:55
L20	9	10/714519	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/11/09 22:57
L21	50	L13 or L16	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2008/11/09 22:59

L23	39	L21 (monitor\$4)same (mode or state)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:59
L24	21	L21 (monitor\$4)same (mode or state).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 22:59
L25	15	L21 (flush\$4 or eras\$4 or bank)same(memory or buffer or register or storage or table).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:01
L26	8	L24 L25	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:01
L27	28	L24 or L25	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:01
L28	8	26(exception)same (vector)near(table)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:01
L29	8	L26 (secure)same(non \$secure or insecure) same(mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:02
L30	8	L28 L29	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:02
L31	20	L21 (monitor\$4)same (mode).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:02
L32	20	L31(secure)same(non \$secure or insecure) same(mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:02
L33	1	(US-7120771-\$).did.	USPAT	AND	ON	2008/11/09 23:03
L34	1	L33 (flush\$4 or eras\$4 or bank)same(memory or buffer or register or storage or table)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	AND	ON	2008/11/09 23:04

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DH Mansell, MR Nonweiler, PG Middleton - US Patent 7,171,539, 2007 - Google Patents

... Robert Nonweiler, Cambridge (GB); Peter Guy Middleton, Mougins (FR) (73) Assignee:

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... (73) Assignee: ARM Limited, Cambridge ... between a secure mode and a non- secure mode

under control ... at a location specified by an exception vector associated with ...

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... (73) Assignee: ARM Limited, Cambridge (GB) ... EXTERNAL PIN FIG. 16 INSTRUCTION ATTEMPTING

GPRS -> MONITOR ? GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...

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... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING CPRS ->

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... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS ->

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AD Tune, PJ Aldworth, SC Watt, L Beinet, DH ... - US Patent 7,149,862, 2006 - Google Patents

... (73) Assignee: ARM Limited, Cambridge (GB) ... GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE

MODE MONITOR MODE (INTERRUPTS DISABLED) TASK A < TASK A< SMI ...

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SC Watt, L Beinet, DH Mansell, N Chaussade, PG ... - US Patent 7,305,534, 2007 - Google Patents

... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS -> MONITOR ? GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...

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P Wilson, A Frey, T Mihm, D Kershaw, T Alves - IEEE Design & Test of Computers, 2007 - doi.ieeecomputersociety.org

... ARM TrustZone technology builds on the standard user-privilege ... From the nonsecure state, the CPU can enter ... through monitor mode when an exception is trapped ...

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Virtual machines for distributed real-time systems

M Cereia, IC Bertolotti - Computer Standards & Interfaces, 2007 - Elsevier

... the sixth version of the ARM architecture and ... enters the monitor mode from the non-secure state through ... In particular, several exception sources (IRQ, FIQ, and ...

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Key authors: S Ravi - A Raghunathan - S Watt - P Karger - S Chakradhar

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Method and apparatus for secure execution of software prior to a computer system being powered down ... - all 5 versions »

MF Angelo, CA Miller - US Patent 5,850,559, 1998 - freepatentsonline.com

... of the invention utilizes a hash table 206 containing ... on/off switch 182, the interrupt vector points to ... power supply 180 following the secure shutdown procedure ...

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Method and system for executing programs using memory wrap in a multi-mode microprocessor - all 3 versions »

J Letwin - US Patent 5,561,788, 1996 - Google Patents

... a segment descriptor from a descriptor table in the ... the present invention for handling vector interrupts ... three separate protection violations in protected mode. ...

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Method and apparatus for protecting flash memory - all 7 versions »

PE Mattison - US Patent 6,363,463, 2002 - freepatentsonline.com

... DOS programs is to modify the interrupt vector table to intercept ... system initialization process, the reset vector goes in ... to change into a secure operating mode ...

Cited by 23 - Related Articles - Cached - Web Search

Experience with TCP/IP networking protocol S/W over embedded OS for network appliance - all 3 versions »

SW Tak, JM Son, TK Kim - Proceedings of International Workshops on Parallel ..., 1999 - doi.ieeecomputersociety.org

... to enter kernel mode from user mode used in 4.4 ... of interrupt level in order to secure data integrity ... card device driver into the interrupt vector table in the ...

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Secure communication system - all 8 versions »

S Dimoultsas, RJ Ragland, F Hemmati - US Patent 5,963,621, 1999 - freepatentsonline.com

... 32 is a table for describing the Tone Index ... is neither decrypted, nor descrambled (with the exception of certain ... from the POT voice to the secure mode can, and ...

Cited by 23 - Related Articles - Cached - Web Search

Secure power supply for protecting the shutdown of a computer system - all 3 versions »

A Crisan - US Patent 5,751,950, 1998 - freepatentsonline.com

... routine in a system interrupt handling table only if ... shows a second embodiment of the secure power supply ... 174 responds by providing the interrupt vector to the ...

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Making Home Automation Communications Secure - all 7 versions »

P Bergstrom, K Driscoll, J Kimball - 2001 - doi.ieeecomputersociety.org

... Table 1. Communications security layer resource constraints ... The initialization vector for this message includes ... safety-critical, and secure systems' architecture ...

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Exception response table in environment services patterns - all 2 versions »

US Patent 6,339,832, 2002 - freepatentsonline.com

... a program (the polymorphic exception handler) with ... calculating a mathematical table, or solving ... distributed, interpreted, robust, secure, architecture-neutral ...

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Computer emulator - all 2 versions »

H Ogata, A Tanimoto, Y Nakacka, M Kojima, Y ... - US Patent 5,758,124, 1998 - freepatentsonline.com

... Hence, it is not necessary to secure the address in advance. ... Following the step described above, corresponding interrupt vector setting table JT is ...

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Safe and protected execution for the Morph/AMRM reconfigurableprocessor - all 13 versions »

AA Chien, JH Eyun - Field-Programmable Custom Computing Machines, 1999, FCCM'99. ..., 1999 -

ieeexplore.ieee.org

... bus or defeating the tinier interrupt which ensures ... processes run in an unprivileged mode (user mode). The page tables, mapping information for each process ...

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DH Mansell, MR Nonweiler, PG Middleton - US Patent 7,171,539, 2007 - Google Patents

... memory management unit is then operable to cause predetermined tables in the ... GENERATE CPDR VIOLATION EXCEPTION ... NON-SECURE MODE MONITOR MODE (INTERRUPTS ENBLED) ...

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SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,305,712, 2007 - Google Patents

... a secure mode and a non-secure mode under control ... specified by an exception vector associated with ... SUPERVISOR MODE MONITOR MODE / UNDEF MODE SUPERVISOR MODE ...

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... table base address register and a secure translation table base address ... GENERATE CPDR VIOLATION EXCEPTION ... NON-SECURE MODE MONITOR MODE (INTERRUPTS ENBLED) ...

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... the rich operating system controls the normal vector table. From the nonsecure state, the CPU can enter the ... through monitor mode when an exception is trapped ...

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L. Beinet, DH Mansell, SC Watt - US Patent 7,165,159, 2007 - Google Patents

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... of this register to locate the exception vector table whenever the ... Yet another exception

table is used for the exceptions ... the secure and the non-secure states, ...

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F Dahan, C Roussel, A Chateau, P Cumming - US Patent 7,237,061, 2007 - Google Patents

... EXIT STATUS"EXCEPTION" SET RETURN POINTER ... RETURN TO NON- SECURE OPERATION . 2. 031 1032 1034 ... vector table and interrupt service routines are not trusted, ...

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[Xen on ARM: System Virtualization Using Xen Hypervisor for ARM-Based Secure Mobile Phones](#)

JY Hwang, SB Suh, SK Heo, CJ Park, JM Ryu, SY Park ... - Consumer Communications and Networking Conference, 2008. ..., 2008 - [ieeexplore.ieee.org](#)

... Secure and nonsecure guest Linux virtual machines are ... handling that makes CPU to jump into exception vector table. ... sensitive registers such as ARM's FAR ...

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... ARM TrustZone technology builds on the standard user ... the rich operating system controls the normal vector table. ... monitor mode when an exception is trapped into ...

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... ARM Limited, Cambridge (GB) ... SECURE TNON-SECURE PAGE TABLE WALK II MAIN TUB CONTAINS THE VALID TAGGED SECURE DESCRIPTOR ... GENERATE GPRS VIOLATION EXCEPTION ...

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